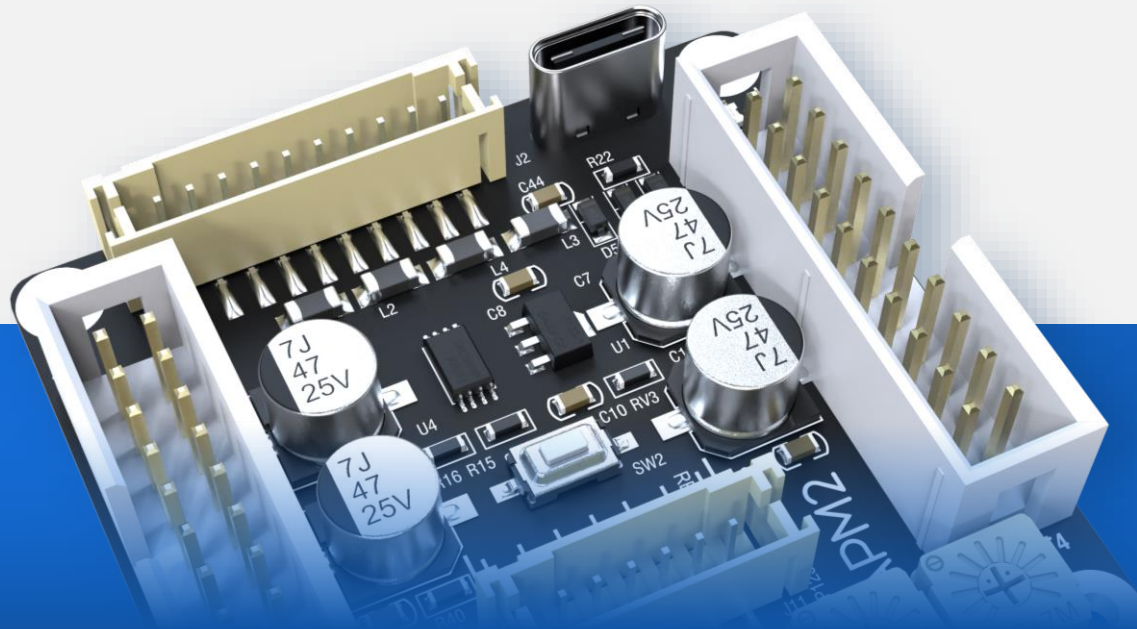


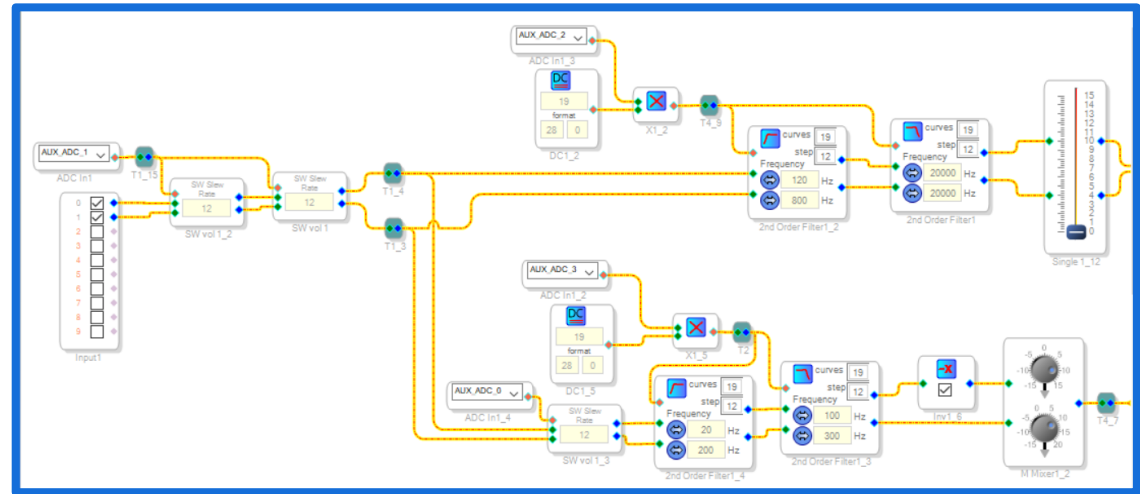
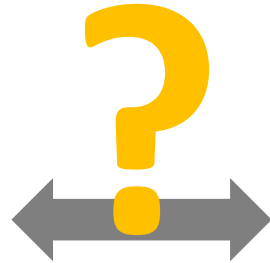
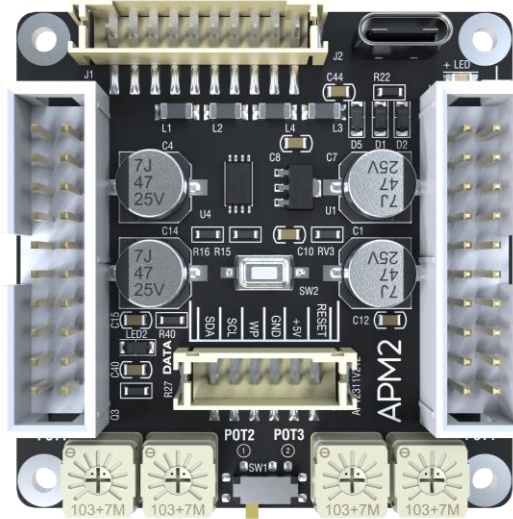
“ The Correspondence of APM2 Hardware & DSP Program



Overview

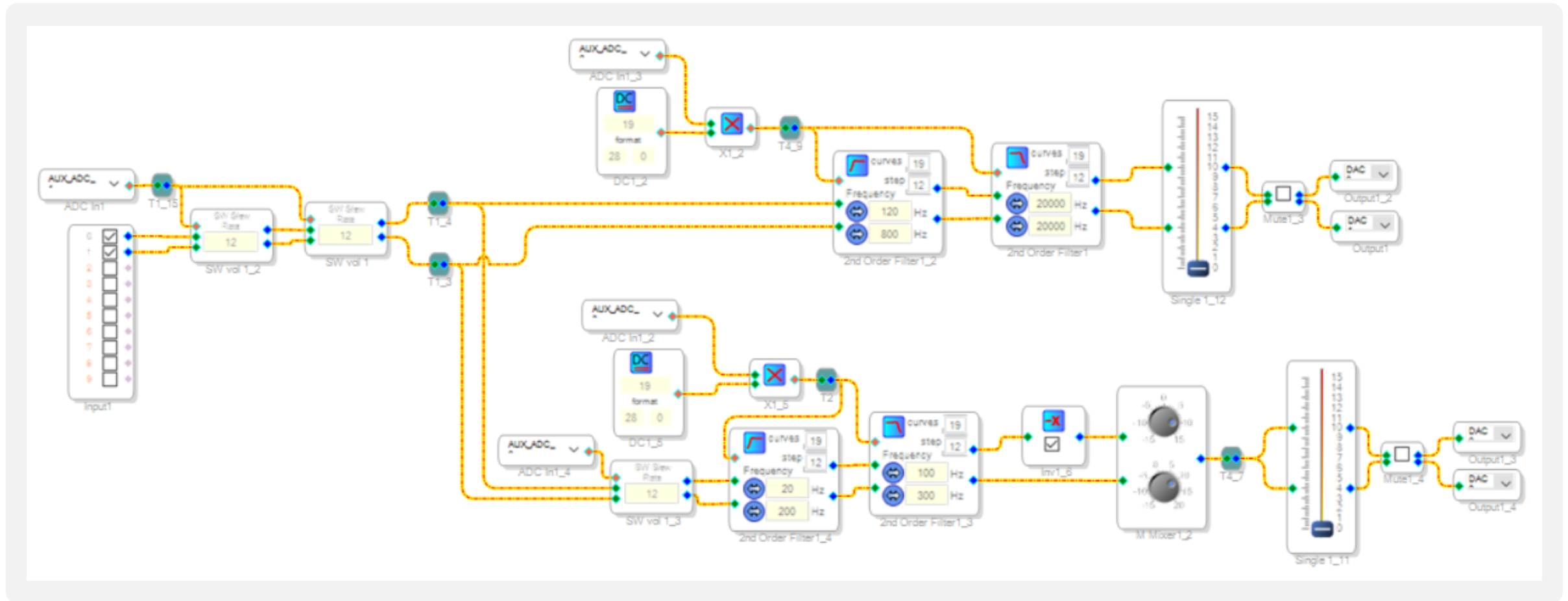
APM2 is the kernel board based on ADAU1701 DSP, which can provide 2-in, 3-out after connection with the interface extension board APM3, suitable for audio 2.1 system and digital crossover applications. Thanks to the integrated debug port, APM2 supports programming through SigmaStudio, which improves the flexibility and expandability. You can program APM2 with original USBi, or WONDOM in-circuit programmer – ICP series.

For customers convenient connection and operation, we developed APM2 with various hardware resources like audio input, output and control, on the basis of ADAU1701's resources. We need to know the correspondence relationship of APM2 hardware and DSP software, along with the remaining available resources of ADAU1701 for better further development of APM2.



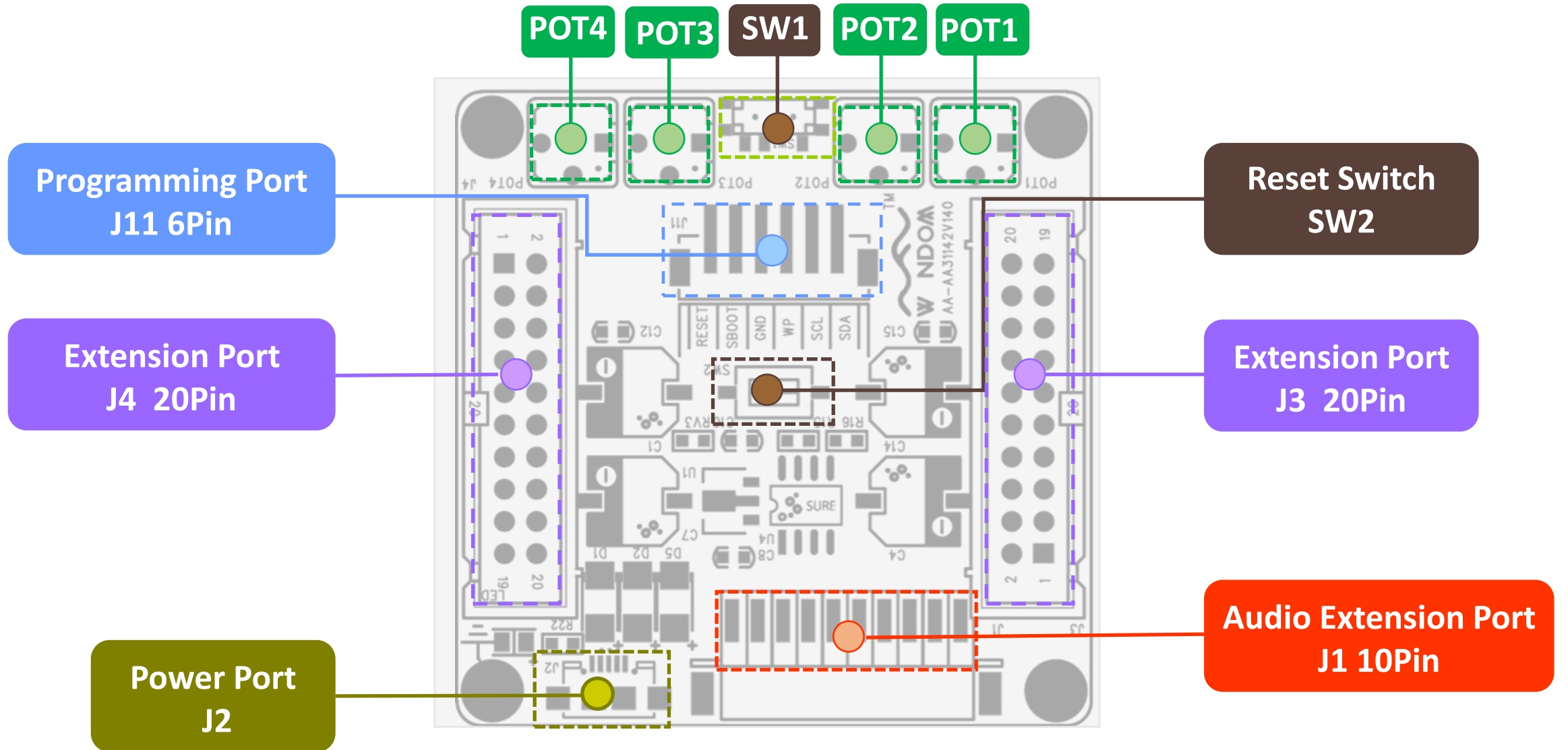
Correspondence Relationship

To make it easier and clearer for your understanding, we will make use of the open-sourced demo program to explain the correspondence relationship of APM2 hardware and ADAU1701 program. You can download the program [HERE](#).





APM2 Interfaces

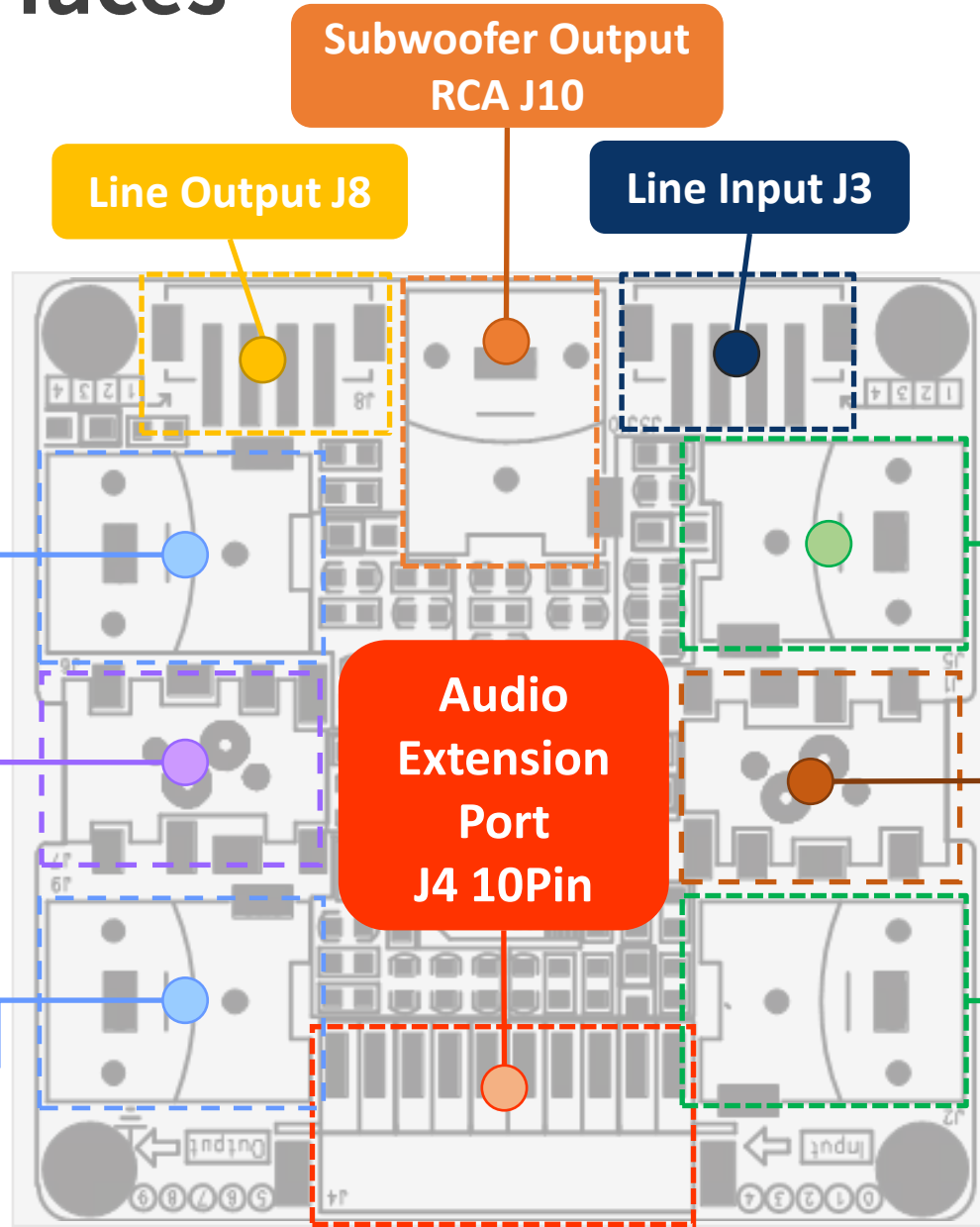




APM3 Interfaces

The stereo output (RCA, headphone & line output) of APM3 is connected in parallel. They cannot be used at the same time.

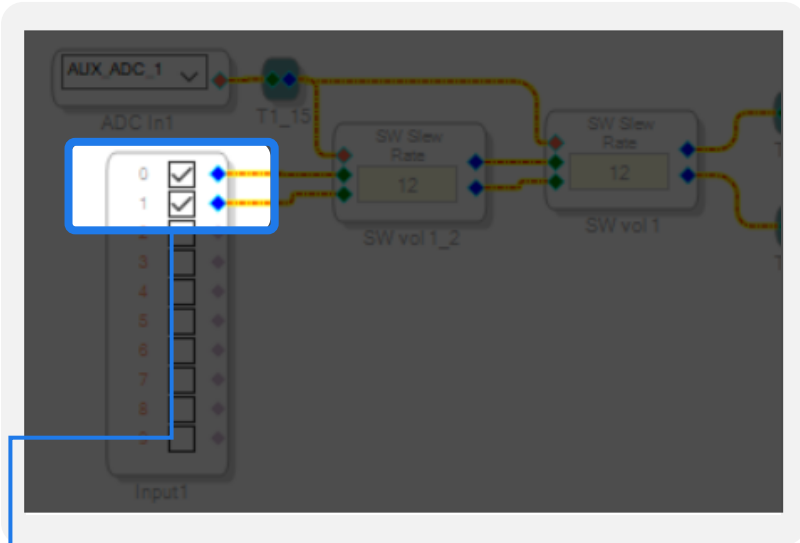
The stereo input (RCA, 3.5mm aux in & line input) of APM3 is connected in parallel. They cannot be used at the same time.





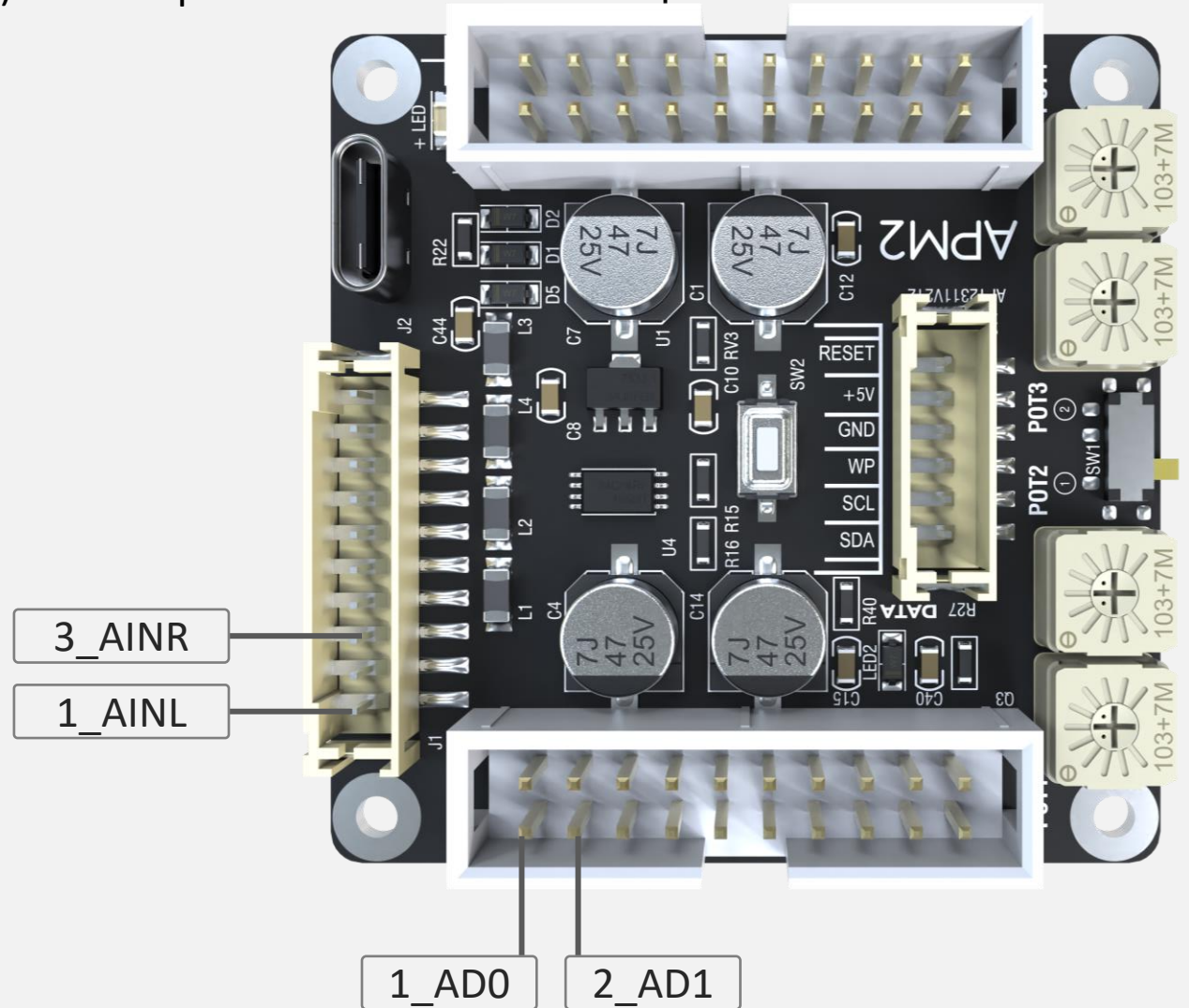
Audio Input

APM2 supports stereo analog input, which in hardware is pin 1 (AINL) & pin 3 (AINR) of J1, and pin 1 (AD0) & pin 2 (AD1). In the demo program, the 0 (ADC_IN0) and 1(ADC_IN1) of the input module is for stereo input.



Analog Input

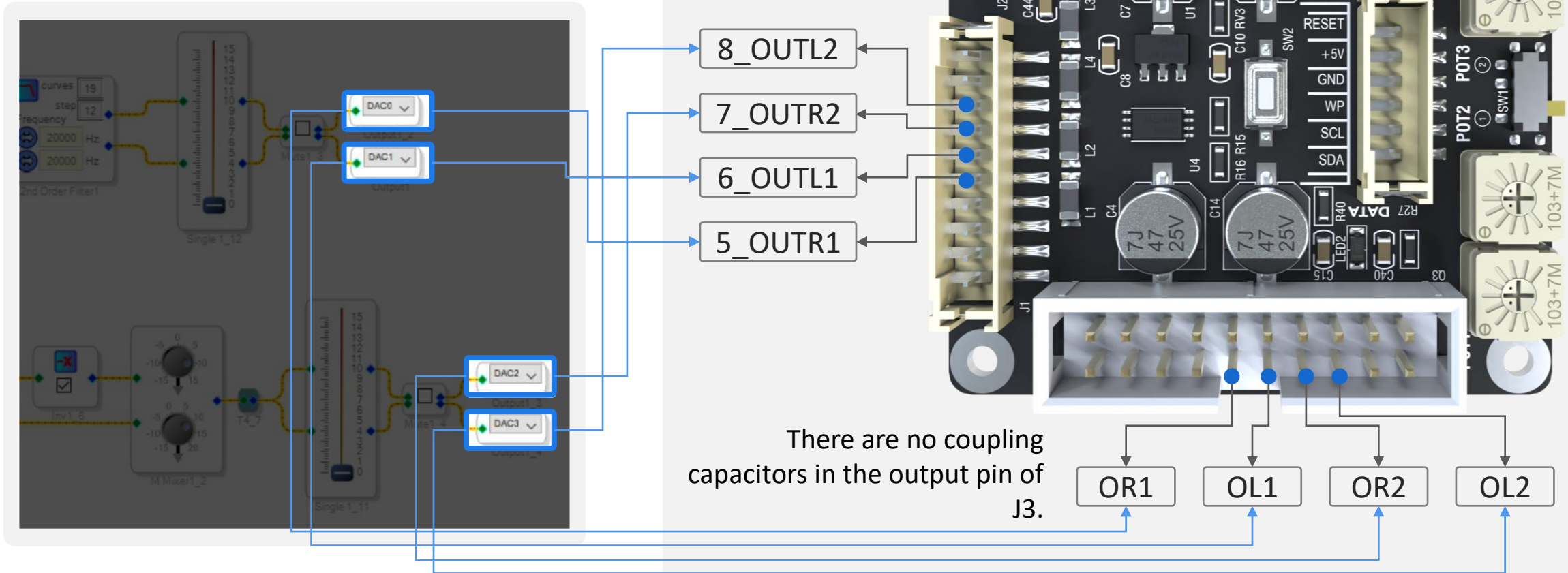
0 (ADC_IN0) and 1 (ADC_IN1) of the input module is for analog input.





Audio Output

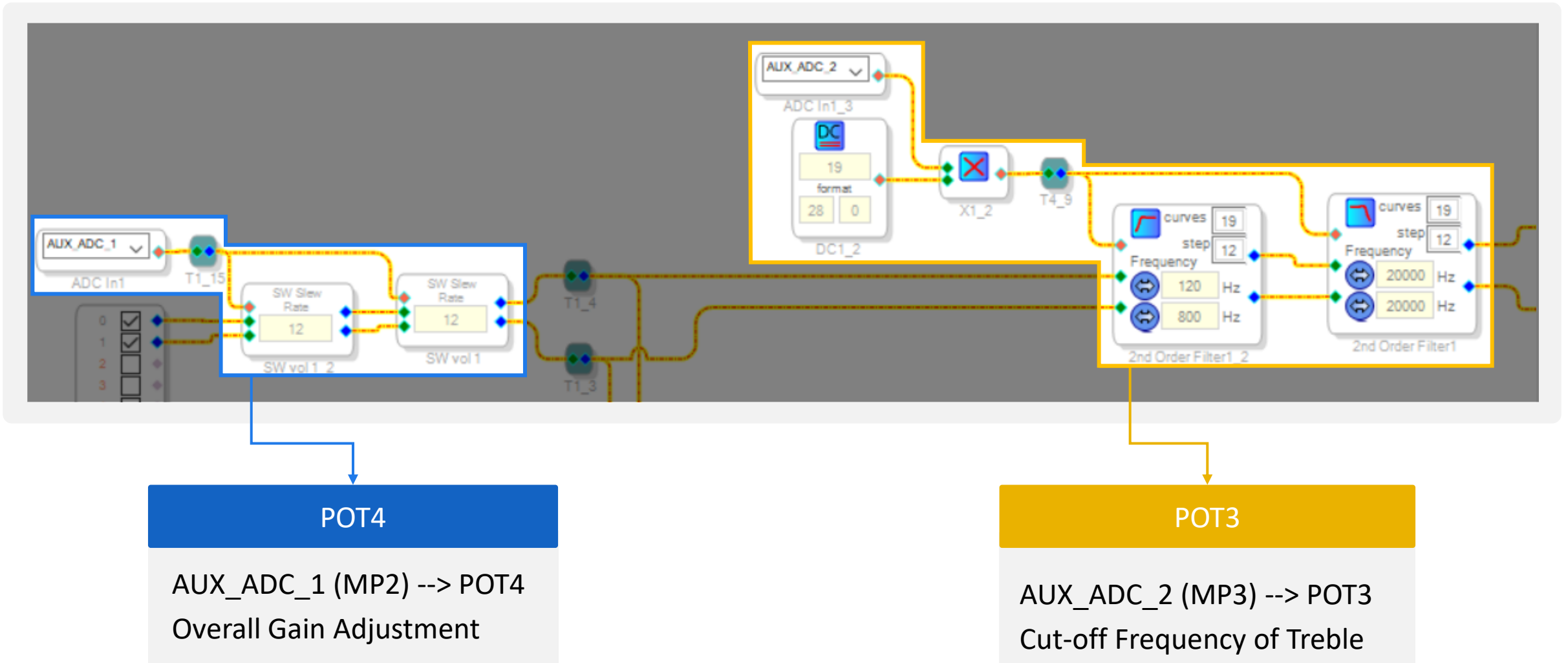
APM2 supports 2-in, 4-out. The output in hardware is pin 5, 6, 7, 8 (OUTR1, OUTL1, OUTR2, OUTL2) of J1 and OR1, OL1, OR2, OL2 pin of J3, which is separately corresponded to DAC0, DAC1, DAC2, DAC3 output module in the program. APM3 interface extension board only supports 2-in, 3-out.





Potentiometers

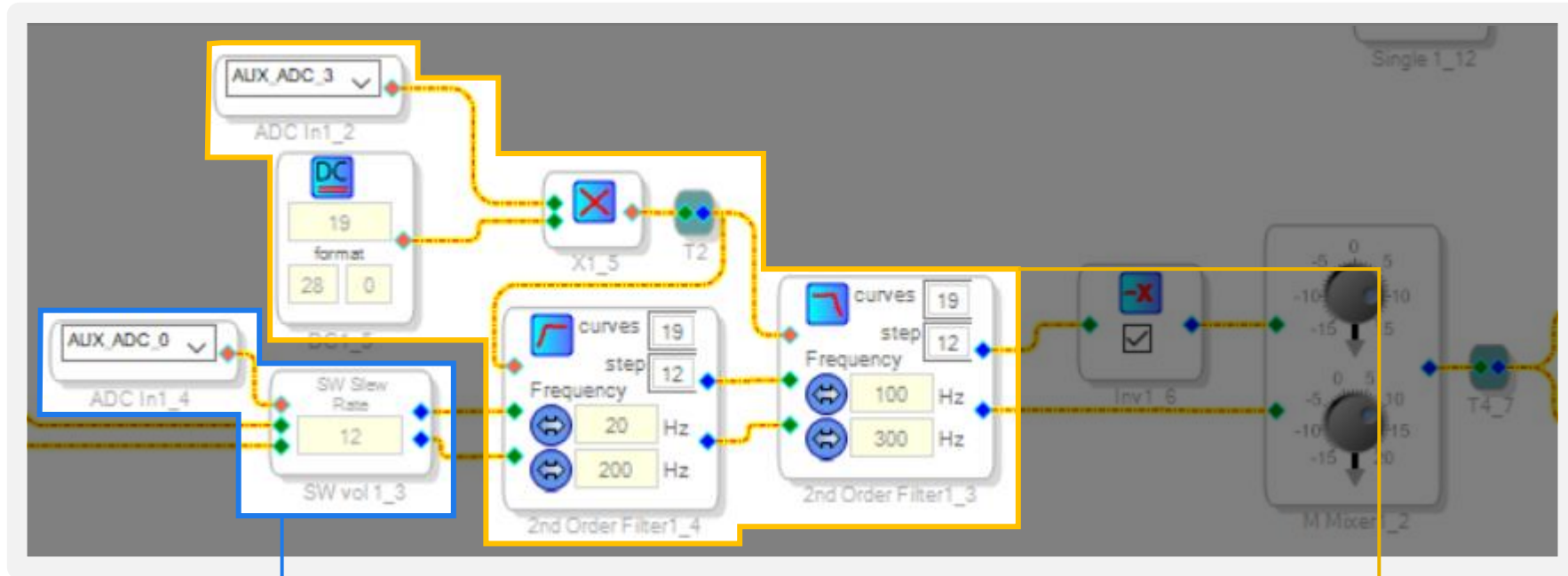
There are four on-board potentiometers on APM3, which can be used to adjust the gain and cut-off frequency of audio system. The mapping relationship is as follows.





Potentiometers

There are four on-board potentiometers on APM3, which can be used to adjust the gain and cut-off frequency of audio system. The mapping relationship is as follows.



POT1
AUX_ADC_0 (MP9) --> POT1
Bass Gain Adjustment

POT2
AUX_ADC_3 (MP8) --> POT2
Cut-off Frequency of Bass

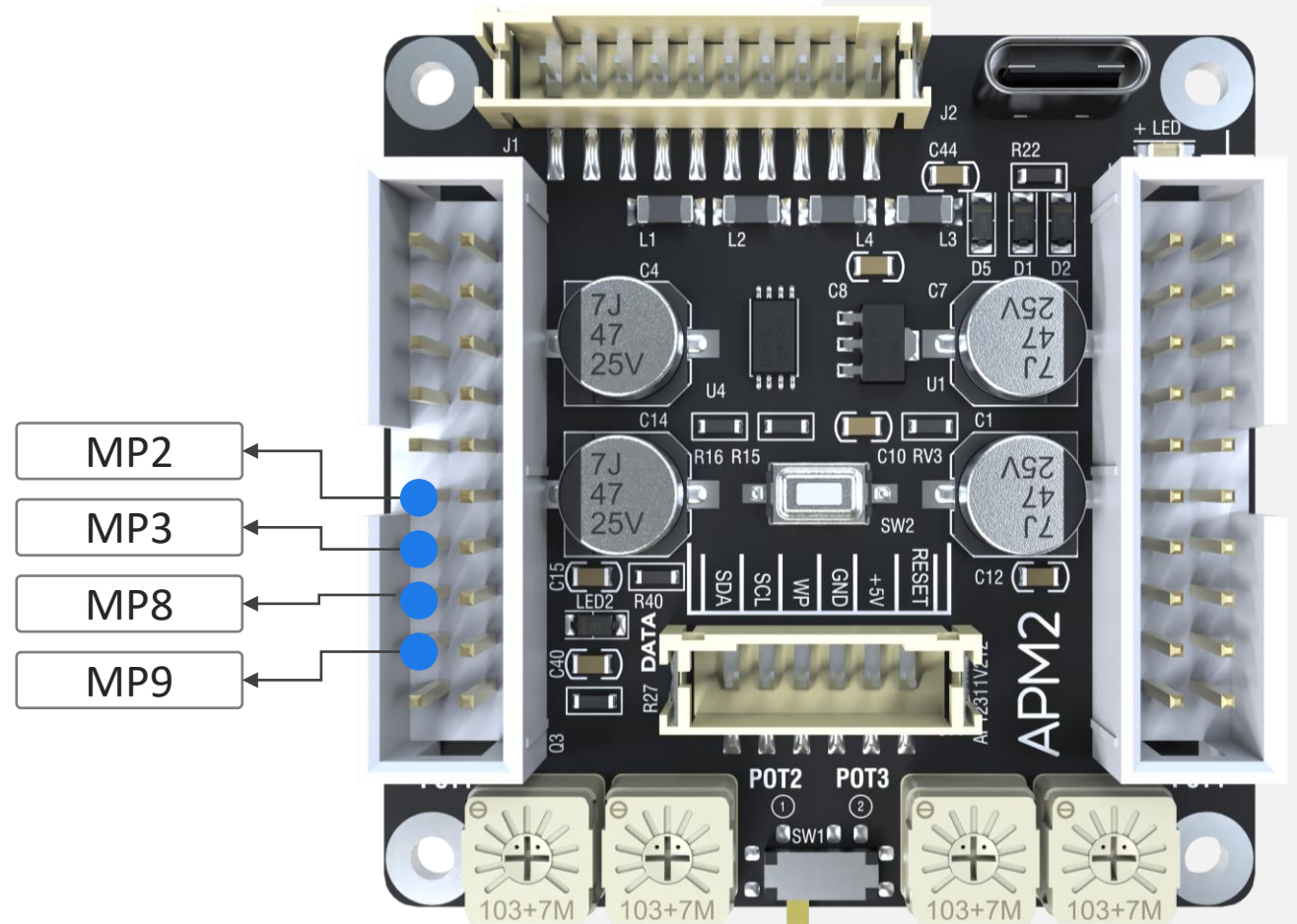


Potentiometers

If you want external potentiometers, you can lead out MP2, MP3, MP8, MP9 of J3.

Lead out +3.3V, GND and corresponding pin of the potentiometer for an external control.

Please note, if you want to adjust audio parameters through the external potentiometers, you need to set the on-board potentiometers at the maximum value at first.



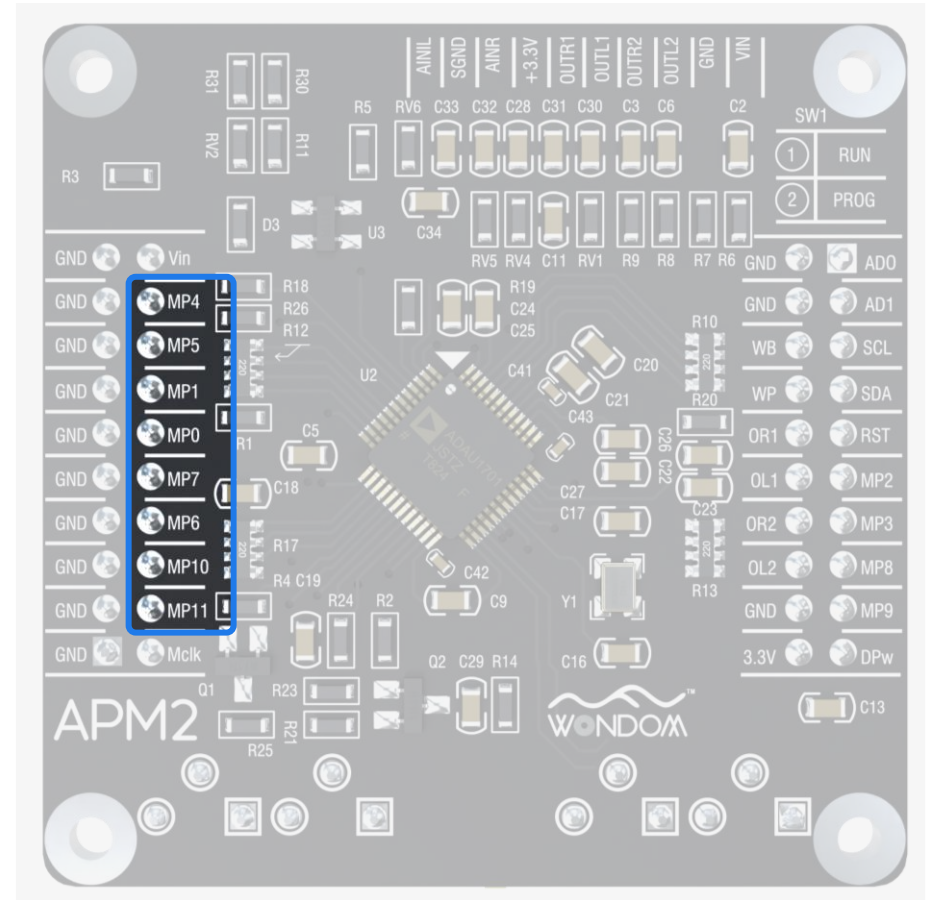


Extension Port

Pin	Value	Direction	Inv
MP0	Low	Input GPIO Debounce	<input type="checkbox"/>
MP1	Low	Input GPIO Debounce	<input type="checkbox"/>
MP2	Low	ADC1	<input checked="" type="checkbox"/>
MP3	Low	ADC2	<input checked="" type="checkbox"/>
MP4	Low	Input GPIO Debounce	<input type="checkbox"/>
MP5	Low	Input GPIO Debounce	<input type="checkbox"/>
MP6	Low	Input GPIO Debounce	<input checked="" type="checkbox"/>
MP7	Low	Input GPIO Debounce	<input type="checkbox"/>
MP8	Low	ADC3	<input checked="" type="checkbox"/>
MP9	Low	ADC0	<input checked="" type="checkbox"/>
MP10	Low	Input GPIO Debounce	<input checked="" type="checkbox"/>
MP11	Low	Input GPIO Debounce	<input checked="" type="checkbox"/>

MP2, MP3, MP8 & MP9 are for potentiometers.

There are two 20-pin extension ports on APM3. ○ MP0, MP1, MP4-MP7, MP10 and MP11 are still available for further development.

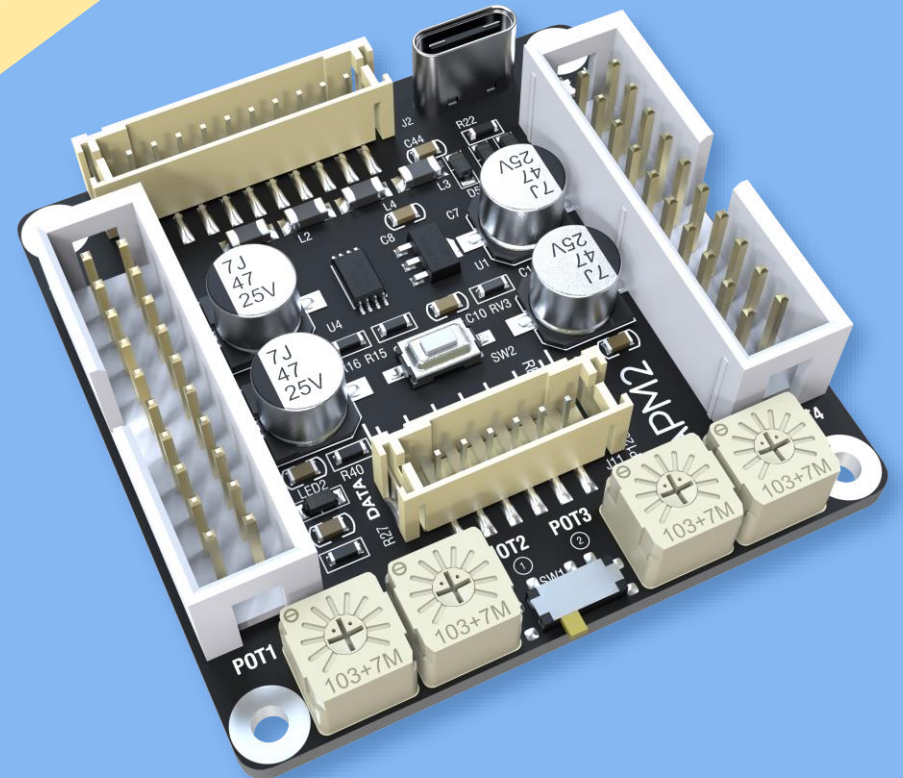


APM2 I2S

Input & Output

When mentioning I2S input and output, we need to identify the master-slave mode of the device and consider the configuration of MCLK.

Therefore, the first step in implementing I2S input or output is to determine the master-slave mode and how MCLK should be configured based on your device. You can perform a self-check using the chart below.

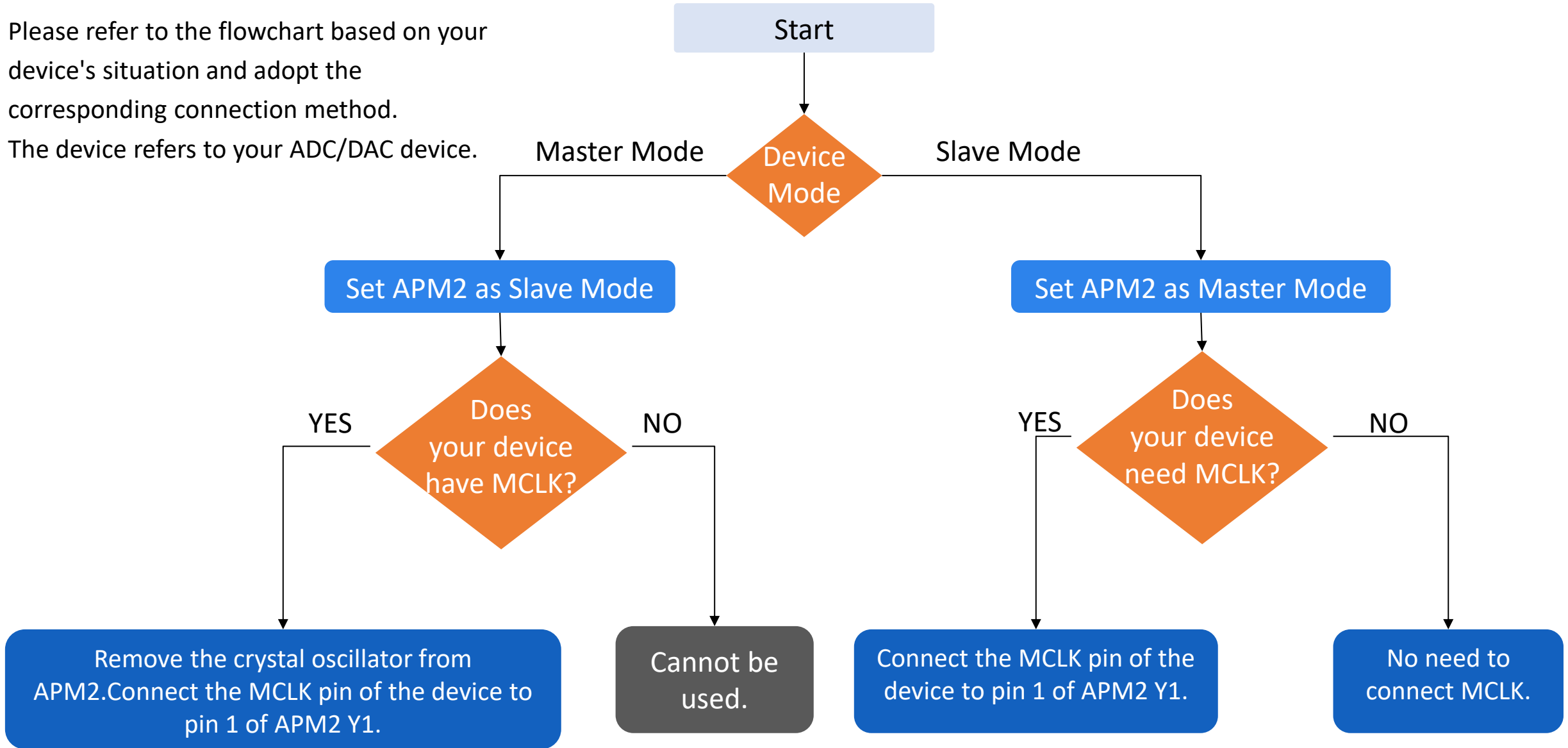




Mode & MCLK Configuration

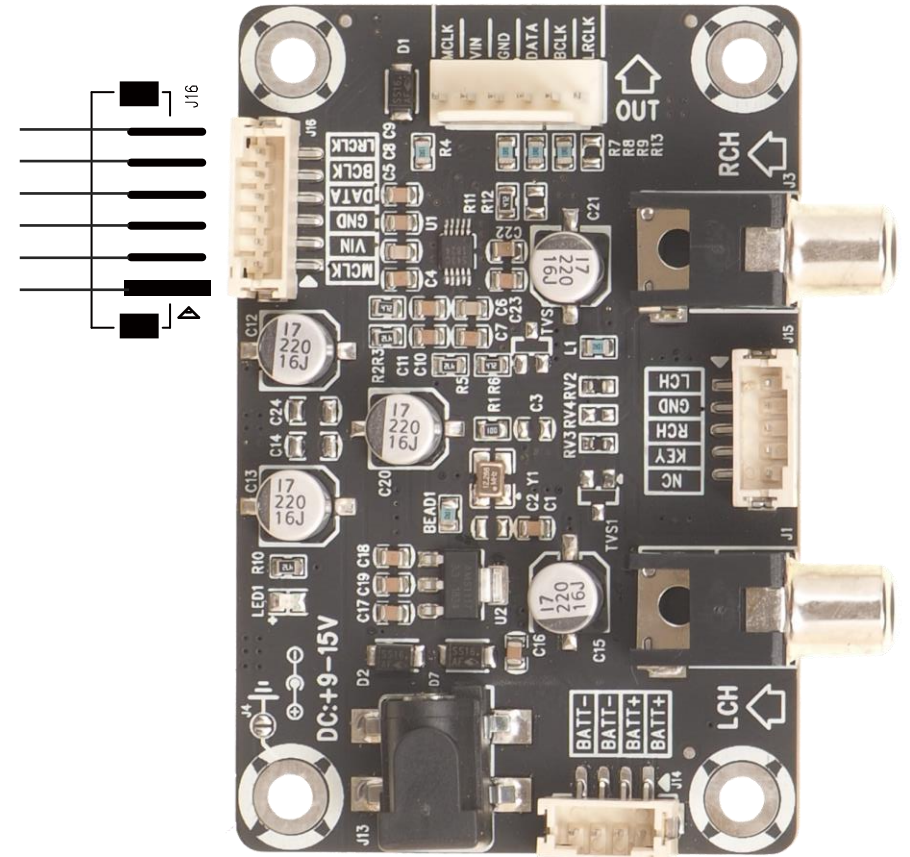
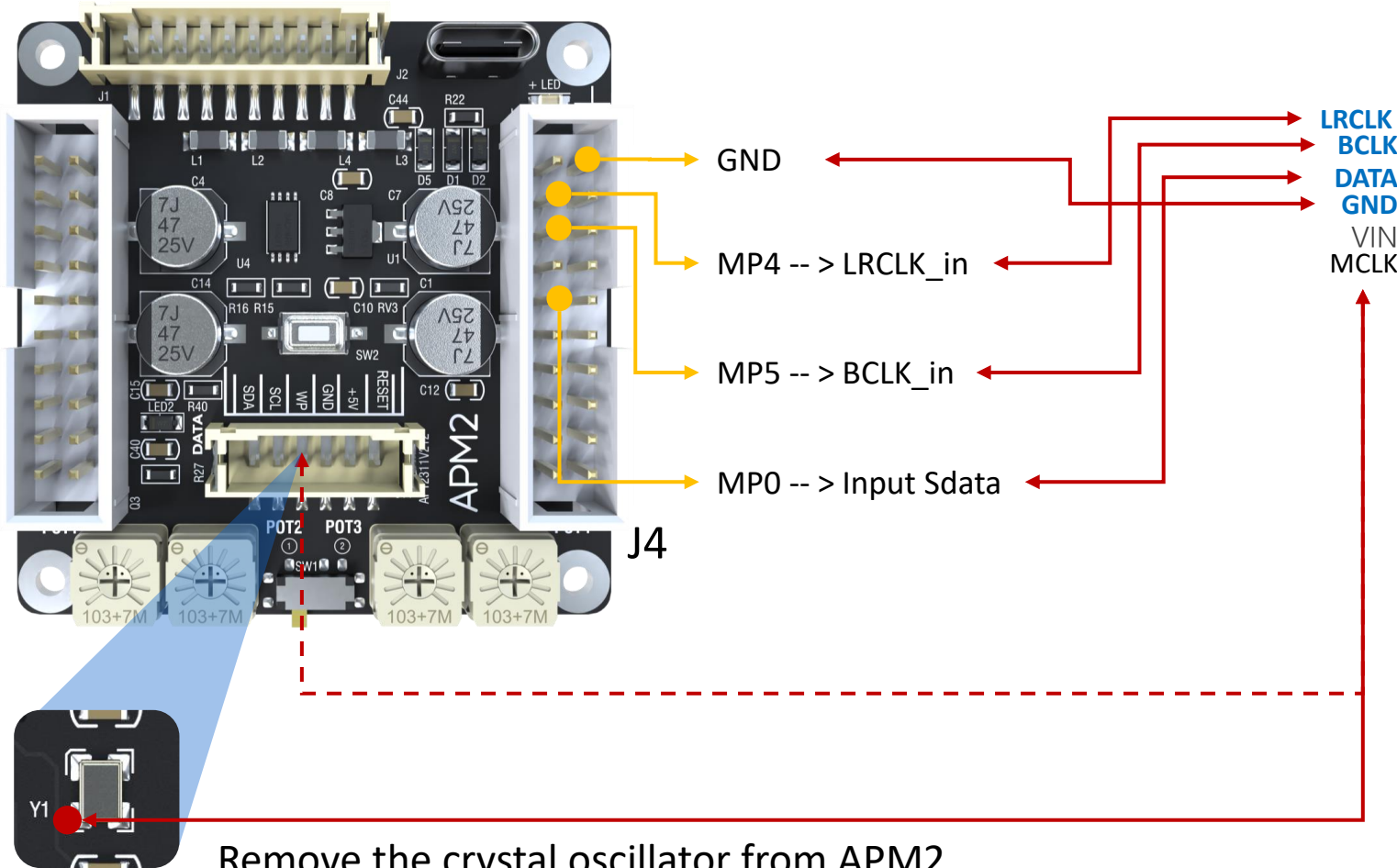
Please refer to the flowchart based on your device's situation and adopt the corresponding connection method.

The device refers to your ADC/DAC device.





Connection Diagram for I2S Input



AA-AB41161
CS5343 Analog to I2S
Decode Board

Program Configuration for I2S Input

MP0 -- > Input Sdata

MP4 -- > LRCLK_in

MP0 -- > Input Sdata

MP4 -- > LRCLK_in

MP5 -- > BCLK_in

The screenshot shows the SigmaStudio hardware configuration interface. The 'Serial Input' section is set to 'I2S'. The 'GPIO' table shows the following configurations:

Pin	Value	Direction	Inv
MP0	Low	Input Sdata_in0	<input type="checkbox"/>
MP1	Low	Input GPIO Debounce	<input checked="" type="checkbox"/>
MP2	Low	ADC1	<input checked="" type="checkbox"/>
MP3	Low	ADC2	<input checked="" type="checkbox"/>
MP4	Low	Input Lrclk_in	<input type="checkbox"/>
MP5	Low	Input Bclk_in	<input type="checkbox"/>
MP6	Low	Input GPIO Debounce	<input checked="" type="checkbox"/>
MP7	Low	Input GPIO Debounce	<input checked="" type="checkbox"/>
MP8	Low	ADC3	<input checked="" type="checkbox"/>
MP9	Low	ADC0	<input checked="" type="checkbox"/>
MP10	Low	Input GPIO Debounce	<input checked="" type="checkbox"/>
MP11	Low	Input GPIO Debounce	<input checked="" type="checkbox"/>

The 'Serial Output 1 (channels 0-7)' section shows the following settings:

- Master Mode:
- LRCLK polarity: L R
- Frame Sync Type: LRCLK
- Frame Sync Freq: internal clock/1
- MSB Position: delay by 1
- Word length: 24 bits
- BCLK polarity: L R
- BCLK Frequency: internal clock/1
- TDM Enable:

The 'Register' table shows the following values:

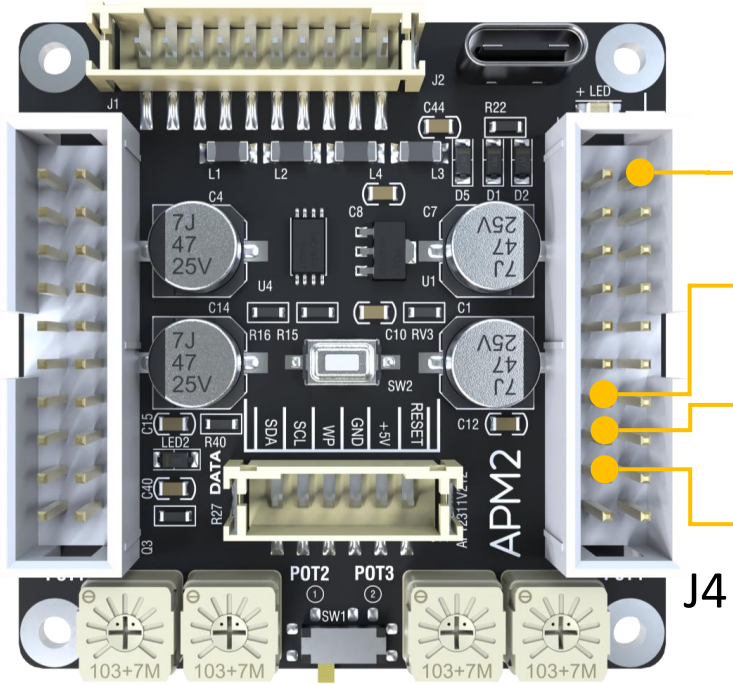
Register	Address	Value
Core	2076	b 00000000011100
Core	2056	b 00000000000000
Core	1000	b 1000
SerialOut1	2078	b 00000000000000
SerialInput	2079	b 000000
MpCfg0	2080	b 010001001111111100000100
MpCfg1	2081	b 1000100011111111100001000
AnalogPower	2082	b 00000000000000
AnalogInterfa	2084	b 100000000000000000
AnalogInterfa	2085	b 0000000000000000

Output

Mode	Time	Cell Name	Parameter Name	Address	Value	Data	Bytes
Block Write	14:16:49 - 385ms	IC 1.CoreRegister	0x081C	0x00, 0x18			2

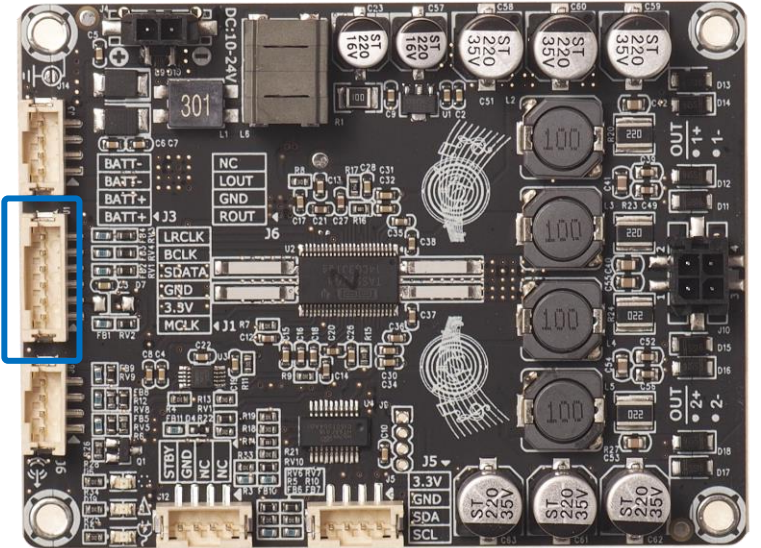
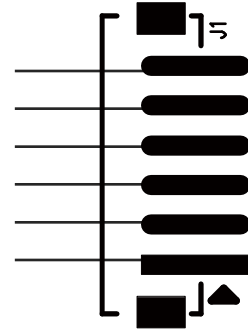


Connection Diagram for I2S Output



- GND
- MP6 --> Output Sdata
- MP10 --> LRCLK_out
- MP11 --> BCLK_out

- LRCLK
- BCLK
- SDATA
- GND
- 3.3V
- MCLK



DIPO1 (AA-AB32255)
2 x 30W - TAS5756

Program Configuration for I2S Output

Pin	Value	Direction	Inv
MP0	Low	Input GPIO Debounce	<input type="checkbox"/>
MP1	Low	Input GPIO Debounce	<input type="checkbox"/>
MP2	Low	ADC1	<input checked="" type="checkbox"/>
MP3	Low	ADC2	<input checked="" type="checkbox"/>
MP4	Low	Input GPIO Debounce	<input type="checkbox"/>
MP5	Low	Input GPIO Debounce	<input type="checkbox"/>
MP6	Low	Output Sdata_out0	<input checked="" type="checkbox"/>
MP7	Low	Input GPIO Debounce	<input type="checkbox"/>
MP8	Low	ADC3	<input checked="" type="checkbox"/>
MP9	Low	ADC0	<input checked="" type="checkbox"/>
MP10	Low	In Lrclk_out	<input checked="" type="checkbox"/>
MP11	Low	In Bclk_out	<input checked="" type="checkbox"/>

MP6 -- > Output Sdata

MP10 -- > LRCLK_out

MP11 -- > BCLK_out

Hardware Configuration Schematic

Serial Input: I2S

LRCLK polarity: [L R]

BCLK data change: [L R]

DSP Core

Program Length: 1x (1024 Instructi...)

RAM Modulo: 8

Zero In/Out Registers

Serial Output 1 (channels 0-7)

Master Mode:

LRCLK polarity: [L R]

Frame Sync Type: LRCLK

Frame Sync Freq: internal clock/1

MSB Position: delay by 1

Word length: 24 bits

BCLK Frequency: internal clock/1

SDATA_OUT1

SDATA_OUT2

SDATA_OUT3

SDATA_OUT0

TDM Enable:

GPIO

Forced By SPI: Debounce: 20ms

Ctrl_IN0: Control ADC

Ctrl_IN1: Enable

Ctrl_IN2: Input Filter

IC 1 - 170x\140x Register Control

IC 2 - WinE2PromLoader

Capture

Mode	Time	Cell Name	Parameter Name	Address	Value	Data	Bytes
Block Write	10:23:37 - 422ms	IC 1.CoreRegister		0x081C		0x00, 0x18	2

Output: IC 1: Params | IC 2: Params



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